DATA SHEET

TDA10045H
DVB-T channel receiver

Product specification
Supersedes data of 2000 Jun 21
File under Integrated Circuits, IC02

2001 Nov 08

Philips
Semiconductors

PHILIPS

DVB-T channel receiver TDA10045H

FEATURES

- 2 and 8 kbytes Coded Orthogonal Frequency Division Multiplexer (COFDM) demodulator (fully DVB-T compliant: ETSI 300-744)
- All modes supported, including hierarchical modes
- Fully automatic transmission parameters detection (including Fast Fourier Transformer (FFT) size and guard interval)
- Digital Signal Processor (DSP) based synchronization (software can be upgraded on the fly)
- No extra-host software required
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 2nd or 1st IF variable analog input
- Only fundamental crystal oscillator required (4 MHz typical ±100 ppm)
- 6, 7 and 8 MHz channels with the same crystal
- Pulse killer algorithm to protect against impulse noise
- Digital frequency correction (±90 kHz)
- Frequency offset ($\pm^1/_6$ MHz) automatic estimator to speed-up the scan
- RF tuner input power measurement
- Parallel or serial transport stream interface
- BER measurement (before and after Viterbi decoder)
- Signal-to noise ratio estimation
- Constellation, CSI and channel frequency response outputs
- TPS bits I²C-bus readable (including spare ones)
- Controllable dedicated I²C-bus for the tuner (5 V tolerant)
- 3 low frequency spare DACs and 2 spare inputs
- CMOS 0.2 μm technology.

APPLICATIONS

- DVB-T fully compatible
- Digital data transmission using COFDM modulation.

GENERAL DESCRIPTION

The TDA10045H is a single-chip channel receiver for 2 and 8 kbytes COFDM modulated signals based on the ETSI specification (ETSI 300-744). The device interfaces directly to an IF signal, which could be either 1st or 2nd IF and integrates a 10-bit Analog-to-Digital Converter (ADC), a Numerically Controlled Oscillator (NCO) and a Phase-Locked Loop (PLL), simplifying external logic requirements and limiting system costs.

The TDA10045H performs all the COFDM demodulation tasks from IF signal to the MPEG-2 transport stream. An internal DSP core manages the synchronization and the control of the demodulation process, and implements specially developed software for robustness against co-channel and adjacent channel interference, to deal with Single Frequency Network (SFN) echo situations, and to assist in a very fast scan of the bandwidth. After baseband conversion and FFT demodulation, the channel frequency response is estimated, which is based on the scattered pilots, and filtered in both time and frequency domains. This estimation is used as a correction on the signal, carrier by carrier. A common phase error and estimator is used to deal with the tuner phase noise. The Forward Error Correction (FEC) decoder is automatically synchronized by the frame synchronization algorithm that uses the TPS information included in the modulation. An embedded ‘pulse killer’ algorithm enables the bad effects of short and strong impulsive noise interference that could be caused by electrical domestic devices and/or car traffic to be greatly reduced.

This device is controlled via an I²C-bus (master). The chip provides 2 switchable I²C-buses derived from the master: a tuner I²C-bus to be disconnected from the I²C-bus master when not necessary and an EEPROM I²C-bus. The DSP software code can be fed to the chip via the master I²C-bus or via the dedicated EEPROM I²C-bus.

Designed in 0.2 μm CMOS technology and housed in a 100 pin QFP package, the TDA10045H operates over the commercial temperature range.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		VERSION
	NAME	DESCRIPTION	
TDA10045H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

BLOCK DIAGRAM

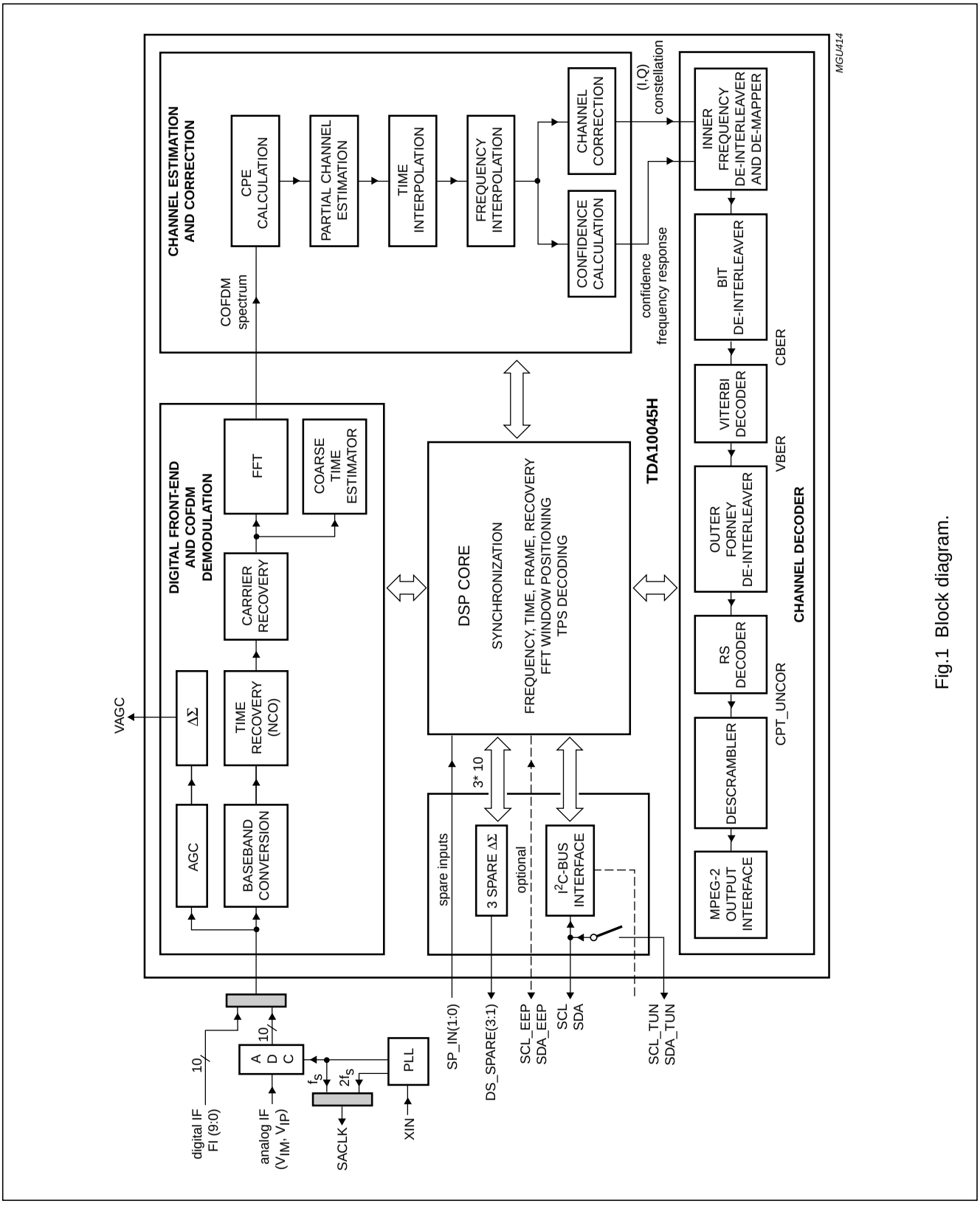


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{DDD33}	1	–	digital supply voltage for the pads (3.3 V typ.)
V_{SSD}	2	–	digital ground supply (0 V
DS_SPARE3	3	O	spare delta-sigma output; managed by the DSP to generate an analog level (after a RC low-pass filter)
VAGC	4	O	output value from the Delta-Sigma modulator, used to control a log-scaled amplifier (after analog filtering)
SCL_EEP	5	O	extra I^2C-bus clock to download DSP code from an external EEPROM (optional mode); can be connected to the master I^2C-bus
V_{DDD33}	6	–	digital supply voltage for the pads (3.3 V typ.)
V_{SSD}	7	–	digital ground supply (0 V)
SDA_EEP	8	I/OD	extra I^2C-bus data bus to download DSP code from an external EEPROM (optional mode). It can be connected to the master I^2C-bus; this pin is open-drain which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50}), even if not used.
SCL_TUN	9	OD(1)	tuner I^2C-bus serial clock signal; this signal is derived from the master SCL and is open-drain which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50}), even if not used
SDA_TUN	10	I/OD	tuner I^2C-bus serial data signal; this signal is derived from the master SDA and is open-drain which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50}), even if not used
SCL	11	I(2)	I^2C-bus master serial clock; up to 700 kbit/s
SDA	12	I/OD	I^2C-bus master serial data input/output, open-drain I/O pad, which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50})
n.c.	13	–	not connected
CLR#	14	I(2)	asynchronous reset signal; active LOW
EEPADDR	15	I(2)	EEPADDR is the LSB of the I^2C-bus address of the EEPROM. The MSBs are internally set to 101000. Therefore the complete I^2C-bus address of the EEPROM is (MSB to LSB): 1, 0, 1, 0, 0, 0, EEPADDR.
SADDR[1:0]	16 and 17	I(2)	SADDR[1:0] are the 2 LSBs of the I^2C-bus address of the TDA10045; the MSBs are internally set to 00010; therefore the complete I^2C-bus address of the TDA10045 is (MSB to LSB): 0, 0, 0, 1, 0, SADDR[1] and SADDR[0]
V_{DDD18}	18	–	digital supply voltage for the core (1.8 V typ.)
V_{SSD}	19	–	digital ground supply (0 V)
TM[3:0]	20 to 23	I(2)	test mode bus; for test purpose; must be set to ‘0000’
SCAN_EN	24	I(2)	scan enable for production test; connected to GND
V_{DDD50}	25	–	digital supply voltage (5 V typ.); can be set to 3.3 V (with caution) if the 5 V tolerant I/O is not required
V_{SSD}	26	–	digital ground supply (0 V)
DWNLOAD	27	I(2)	processor control, boot mode; if set to logic 0, the DSP downloads the software from an external EEPROM on the dedicated I^2C-bus (pins SDA_EEP and SCL_EEP). If set to logic 1 the software is downloaded in the I^2C-bus register CODE_IN from the host; in this case the external EEPROM is not needed.
SP_IN[1:0]	28 and 29	I(2)	spare inputs

SYMBOL	PIN	TYPE	DESCRIPTION
FFT_WIN	30	I/O	output or input signal indicating the start of the active data; equals 1 during complex sample 0 of the active FFT block; can be used to synchronize 2 chips
V_{DDD33}	31	–	digital supply voltage for the pads (3.3 V typ.)
V_{SSD}	32	–	digital ground supply (0 V)
SACLK	33	O	sampling frequency output; this output clock can be fed to an external (10-bit) ADC as a sampling clock; SACLK can also provide twice the sampling clock
FI[9:5]	34 to 38	I/O	input data from an external ADC, FI must be tied to ground when unused, positive notation (from 0 to 1023) or twos complement notation (from −512 to +511). In internal ADC mode, these outputs can be used to monitor extra demodulator output signals (constellation or frequency response).
V_{DDD18}	39	–	digital supply voltage for the core (1.8 V typ.)
V_{SSD}	40	–	digital ground supply (0 V)
FI[4:0]	41 to 45	IO	input data from an external ADC, FI must be tied to ground when unused, positive notation (from 0 to 1023) or twos complement notation (from −512 to +511). In internal ADC mode, these outputs can be used to monitor extra demodulator output signals (constellation or frequency response).
V_{DDD50}	46	–	digital supply voltage (5 V typ.); can be set to 3.3 V (with caution) if 5 V tolerant I/O is not required
V_{SSD}	47	–	digital ground supply (0 V)
IT	48	OD(1)	interrupt line; this output interrupt line can be configured by the I^2C-bus interface. This pin is an open-drain output and therefore requires an external pull-up resistor (to V_{DDD33} or V_{DDD50}).
FEL	49	OD(1)	front-end lock; FEL is an open-drain output and therefore requires an external pull-up resistor (to V_{DDD33} or V_{DDD50})
n.c.	50	–	not connected
n.c.	51	–	not connected
TRSTN	52	I(2)	asynchronous reset signal for boundary scan; connected to GND if not used
TMS	53	I(2)	mode programming signal for boundary scan; connected to GND if not used
TDI	54	I(2)	input port for boundary scan; connected to GND if not used
TCK	55	I(2)	clock signal for boundary scan; connected to GND if not used)
TDO	56	O	output port for boundary scan; not connected if not used
V_{DDD18}	57	–	digital supply voltage for the core (1.8 V typ.)
V_{SSD}	58	–	digital ground supply (0 V)
DS_SPARE2	59	O	spare delta-sigma output; managed by the DSP or by an I^2C-bus register to generate an analog level (after a RC low-pass filter)
DS_SPARE1	60	O	spare delta-sigma output; managed by the DSP to handle a low frequency DAC (automatic first stage tuner AGC measurement or 2nd AGC loop control as examples)
V_{DDD33}	61	–	digital supply voltage for the pads (3.3 V typ.)
V_{SSD}	62	–	digital ground supply (0 V)
UNCOR	63	O	RS error flag, active HIGH on one RS packet if the RS decoder fails to correct the errors
PSYNC	64	O	pulse synchro; this output signal goes HIGH on a rising edge of OCLK when a synchro byte is provided, then goes LOW until the next synchro byte

SYMBOL	PIN	TYPE	DESCRIPTION
DEN	65	O	output data validation signal; active HIGH during the valid and regular data bytes
OCLK	66	O	output clock; OCLK is the output clock for the parallel DO[7:0] outputs
DO[7:5]	67 to 69	O	output data carrying the current sample of the current MPEG2 packet (188 bytes), delivered on the rising edge of OCLK by default when the serial mode is selected. The output data is delivered by DO[0].
V_{DDD18}	70	–	digital supply voltage for the core (1.8 V typ.)
V_{SSD}	71	–	digital ground supply (0 V)
DO[4:0]	72 to 76	O	output data carrying the current sample of the current MPEG2 packet (188 bytes), delivered on the rising edge of OCLK by default when the serial mode is selected. The output data is delivered by DO[0].
V_{DDD33}	77	–	digital supply voltage for the pads (3.3 V typ.)
V_{SSD}	78	–	digital ground supply (0 V)
XIN	79	I[2]	crystal oscillator input pin
XOUT	80	O	crystal oscillator output pin; typically a fundamental crystal oscillator is connected between pins XIN and XOUT
V_{DDD18}	81	–	digital supply voltage for the core (1.8 V typ.)
V_{SSD}	82	–	digital ground supply (0 V)
n.c.	83	–	not connected
$V_{CCD(PLL)}$	84	–	power supply input for the digital circuits of the PLL module (1.8 V typ.)
DGND	85	–	ground return for the digital circuits of the PLL module
n.c.	86	–	not connected
PPLGND	87	–	ground return for the analog circuits of the PLL module
$V_{CCA(PLL)}$	88	–	power supply input for the analog circuits of the PLL module (3.3 V typ.)
V_{SSA3}	89	–	ground return for the analog circuits
V_{DDA3}	90	–	power supply input for the analog circuits; the DC voltage should be 3.3 V
V_{IP}	91	–	positive input to the ADC; this pin is DC biased to half supply through an internal resistor divider (2×20 kΩ resistors). In order to remain in the range of the ADC, the voltage difference between pins V_{IP} and V_{IM} should be between −0.5 and +0.5 V.
V_{IM}	92	–	negative input to the ADC; this pin is DC biased to half supply to remain in the range of the ADC, the voltage difference between pins V_{IP} and V_{IM} should be between −0.5 and +0.5 V through an internal resistor divider (2×20 kΩ resistors)
$V_{ref(neg)}$	93	–	negative reference voltage for the ADC
$V_{ref(pos)}$	94	–	positive reference voltage for the ADC
V_{DDA3}	95	–	power supply input for the analog circuits; the DC voltage should be 3.3 V
V_{SSA3}	96	–	ground return for analog circuits
V_{SSA2}	97	–	ground return for the analog clock drivers
V_{DDA2}	98	–	power supply input for the analog clock drivers; the DC voltage should be 3.3 V
V_{SSA1}	99	–	ground return for the digital switching circuitry
V_{DDD1}	100	–	power supply input for the digital switching circuitry; sensitive to the supply noise; the DC voltage should be 1.8 V

Notes

1. OD are open-drain outputs, so they must be connected to a pull-up resistor to either V_{DDD33} or V_{DDD50}
2. All inputs (I) are TTL, 5 V tolerant, (if V_{DD50} is set to 5 V).
3. Foundry test I/O inputs must be connected to GND.

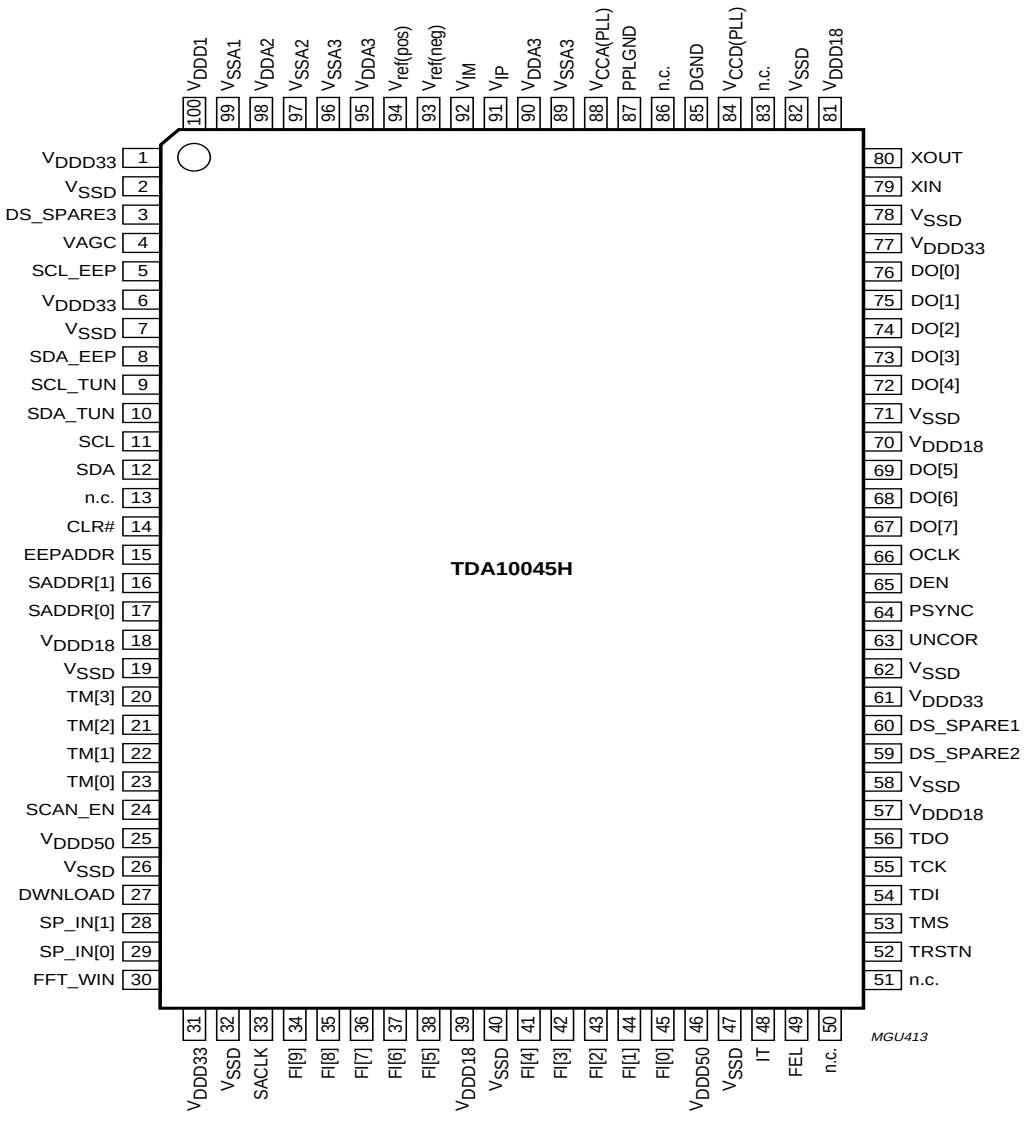


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rate System (IEC 60134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD18}	digital supply voltage for the core	−0.5	+2.1	V
V_{DDD33}	digital supply voltage for the pads	−0.5	+3.8	V
V_I	DC input voltage	−0.5	+5.5	V
I_I	DC input current	–	±20	mA
T_{lead}	lead temperature	–	300	°C
T_{stg}	storage temperature	−65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	0	70	°C

Note

1. Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	tbf	K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Core and pads						
V_{DDD33}	digital supply voltage for the pads	V_{DDD} = 3.3 V ± 10%	2.97	3.3	3.63	V
V_{DDD18}	digital supply voltage for the core	V_{DDD} = 1.8 V ± 5%	1.7	1.8	1.9	V
V_{DDD50}	5 V supply voltage	only for 5 V requirements; note 1	4.75	5.0	5.25	V
T_{amb}	ambient temperature		0	–	70	°C
V_{IH}	HIGH-level input voltage	TTL input; note 2	2	–	V_{DDD50}	V
V_{IL}	LOW-level input voltage	TTL input	0	–	0.8	V
V_{OH}	HIGH-level output voltage	I_{OH} = ±2 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = ±2 mA	–	–	0.4	V
C_i	input capacitance		–	–	5	pF
C_o	output capacitance		–	–	5	pF
PLL						
$V_{CCD(PLL)}$	digital PLL supply voltage	V_{CCD} = 1.8 V ± 5%	1.7	1.8	1.9	V
$V_{CCA(PLL)}$	analog PLL supply voltage	V_{CCA} = 3.3 V ± 10%	2.97	3.3	3.63	V
ADC						
V_{DDD1}	digital ADC supply voltage	V_{DDD} = 1.8 V ± 5%	1.7	1.8	1.9	V
V_{DDA2}, V_{DDA3}	analog ADC supply voltage	V_{DDA} = 3.3 V ± 10%	2.97	3.3	3.63	V
$V_{i(ADC)}$	analog ADC inputs pins V_{IP} and V_{IM}		–0.5	–	V_{DDD3} + 0.5	V
V_i	signal input	$I_R = V_{IP} - V_{IM}$; depending on SW register	–0.5 to –1.0	–	+0.5 to +1.0	V
$V_{ref(pos)}$	positive reference voltage	with SW register = 11	1.95	2.15	2.35	V
$V_{ref(neg)}$	negative reference voltage	with SW register = 11	0.95	1.15	1.35	V
$V_{i(offset)}$	input offset voltage		–25	–	+25	mV
R_i	input resistance pin V_{IP} or V_{IM}		–	10		kΩ
C_i	input capacitance pin V_{IP} or V_{IM}		–	5	10	pF
B_W	input full power bandwidth	3 dB bandwidth	40	50	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power consumption						
I_{DDD}	digital supply current on pins:	f_s = 29 Mhz; direct IF application				
	V_{DDD18} and V_{DDD1}		–	140	160	mA
	V_{DDD33}		–	3	–	mA
	$V_{CCD(PLL)}$, V_{DDA2} and V_{DDA3}		–	35	–	mA
	V_{DDD50}		–	5	–	mA
P_{tot}	total power dissipation		–	400	470	mW

Notes

1. The voltage level of the 5 V supply must always exceed, or at least equal, the voltage level of the 3.3 V supply during power-up and down in order to guarantee protection against latch-up.
2. All inputs are 5 V tolerant.

APPLICATION INFORMATION

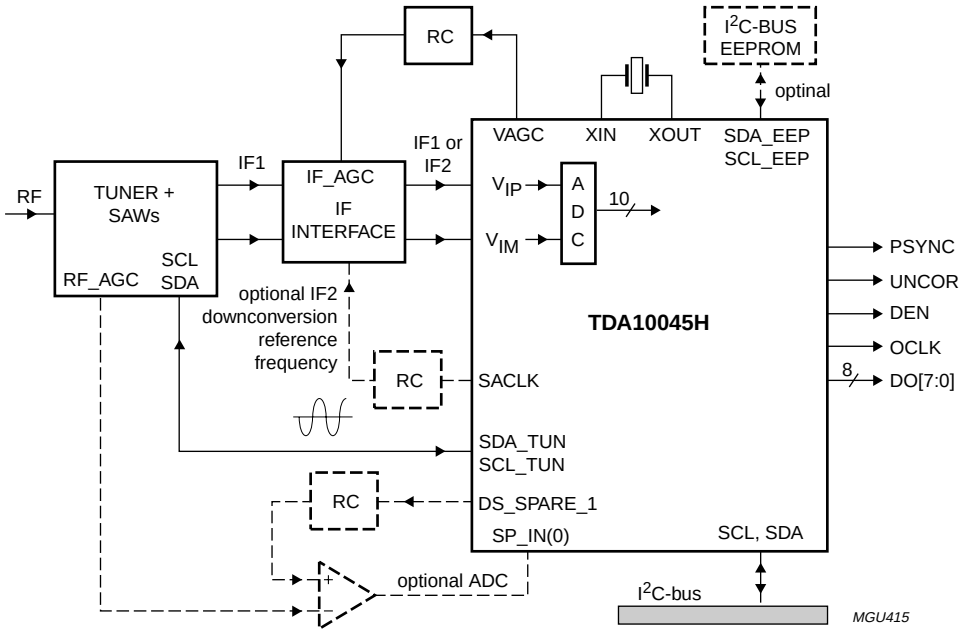


Fig.3 DVB-T front-end receiver.

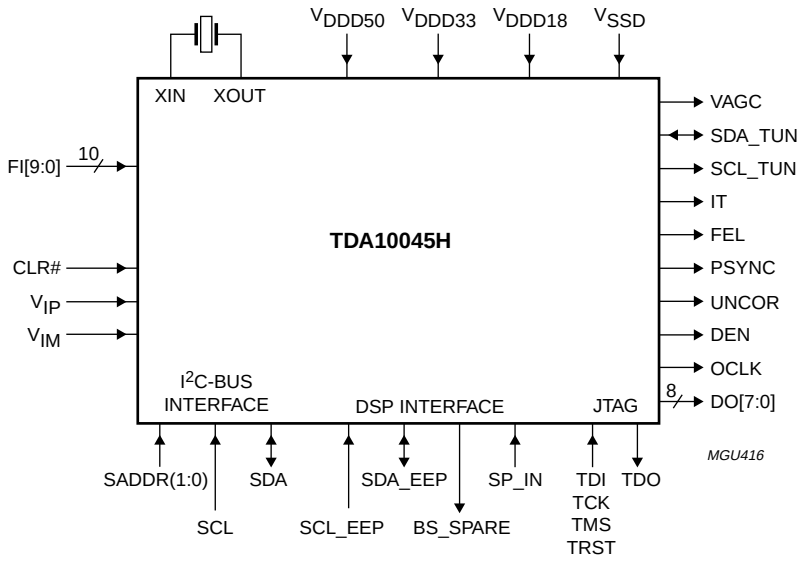


Fig.4 Application diagram.

Tuner

- A RF tracking filter tracks the RF wanted frequency and suppresses the image
- A first local wideband AGC is usually done at RF level, the AGC level information could be provided externally and the chip offers facilities to measure this level by the optional ADC (this measurement is automatically made by the DSP, the host has just to read the result)
- A mixer oscillator and a PLL downconverts the RF signal to intermediate frequency IF1 (36.125 MHz typ.)
- SAW filters eliminate the power of the adjacent channels around IF1.

IF interface

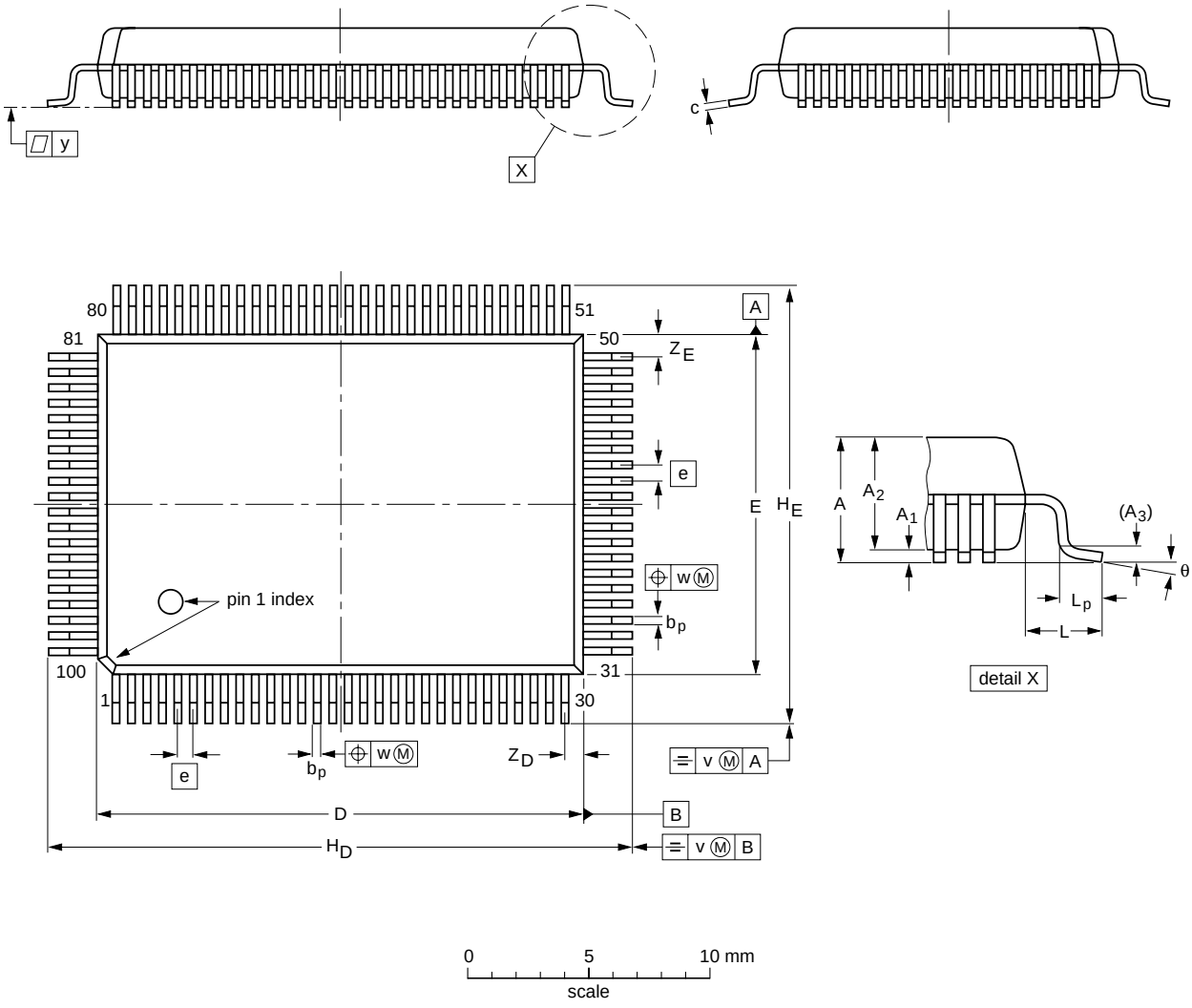
- It is either an analog IF amplifier when IF1 is sampled (direct IF: digital downconversion concept) or an analog IF amplifier followed by a downconversion from IF1 to IF2 at a few MHz (e.g. 4.57 MHz)
- When this second solution is used, the ADC sampling clock could be used (after low-pass filtering) as a reference clock for downconversion (twice the ADC sampling clock could also be provided)
- The IF amplifier is controlled by the digital AGC of the chip. A simple RC circuit filters the single bit ($\Delta\Sigma$ modulated) AGC control (VAGC)
- The sampling clock could also be used to control an external ADC, the inputs to the chip will then be digital (FI[9:0]).

TDA10045H

- The chip is controlled by an I^2C-bus and driven by an external low-cost crystal oscillator
- The software of the embedded DSP can be downloaded from the main I^2C-bus or from a dedicated I^2C-bus connected to an external slave I^2C-bus EEPROM
- An internal bidirectional switch enables the tuner to be programmed through the chip and then switch-off the link in order to avoid phase noise distortions due to I^2C-bus traffic.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2		MO-112				~~97-08-01~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

ICs with MPEG-2 functionality — Use of this product in any manner that complies with the MPEG-2 Standard is expressly prohibited without a license under applicable patents in the MPEG-2 patent portfolio, which license is available from MPEG LA, L.L.C., 250 Steele Street, Suite 300, Denver, Colorado 80206.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands 753504/04/pp20 Date of release: 2001 Nov 08 Document order number: 9397 750 08496

Let's make things better.

Philips
Semiconductors

PHILIPS